AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application:

Listing of Claims:

1. (Currently Amended) A computer implemented interrupt arbitration system, comprising:

at least one request associated with an interrupt resource and a requesting component wanting allocation of the interrupt resource, the request including at least ~~two dimensions related to an interrupt and an interrupt service component, at least one dimension including~~ a requested amount of ~~a resource's~~ time to allocate the interrupt resource to the requesting component; and

at least one arbiter to process the request and return a subset of interrupt resource ranges in view of available system resources.

2. (Currently Amended) The system of claim 1, further comprising the [[a]] requesting component ~~that~~ communicates to the arbiter in order to determine available system resources that may be utilized by the requesting component to perform one or more tasks.

3. (Original) The system of claim 2, the system resources are related to at least one of I/O ports, memory locations, DMA channels (Direct Memory Access), bus numbers, and interrupt requests (IRQs).

4. (Original) The system of claim 3, further comprising at least one arbiter for a respective system resource.

5. (Original) The system of claim 4, the system resources are associated with one or more system devices, buses, or other components which are negotiated for via the at least one arbiter.

6. (Original) The system of claim 2, the requesting component issues a multidimensional interrupt request (IRQ) associated with one or more interrupt inputs, signals, or assignments, the IRQ is employed to interrupt at least one processing component.

7. (Original) The system of claim 1, the interrupt service component is associated with an Interrupt Descriptor Table (IDT) entry that is concurrently mapped with an IRQ.

8. (Original) The system of claim 7, the IRQ is mapped in accordance with a first request and the IDT entry is mapped in accordance with a separate request.

9. (Original) The system of claim 1, the arbiter performs an analysis of system resources, and if requested interrupt resources are found to be available, the arbiter returns a resource subset or data packet indicating the interrupt resources that can be utilized by a requesting component.

10. (Original) The system of claim 9, if the interrupt resources are not deemed available by the arbiter, a code or flag is returned to the requesting component indicating that requested interrupt resources cannot be satisfied.

11. (Previously Presented) The system of claim 1, the request further comprising at least one other dimension including a priority component.

12. (Original) The system of claim 2, the requesting component is a Plug and Play (PnP) manager that communicates with individual plug-in modules which decide which resources can be assigned to specific devices.

13. (Original) The system of claim 12, further comprising a driver that supplies an arbiter to arbitrate interrupts.

14. (Original) The system of claim 13, the arbiter includes an interface associated with a function related to at least one of the following: testing/analyzing whether a possible set of resources operate; committing a specific set of resources that has been requested by a PnP manager; querying for a set of devices that conflict with a resource set; and marking resources that were in use by an operating system component when a machine is booted.

15. (Original) The system of claim 14, the arbiter is associated with a library function.

16. (Original) The system of claim 15, the library function is associated with a FindSuitableRange function that searches across available IRQs and available IDT entries.

17. (Original) The system of claim 1, further comprising a control component to tune performance of a machine by influencing interrupt assignment policy.

18. (Original) The system of claim 17, further comprising a monitor component to provide feedback to the control component regarding system performance.

19. (Original) The system of claim 1, the interrupt is a Message-Signaled Interrupts (MSI).

20. (Original) The system of claim 1, further comprising at least one of the following Application Programming Interfaces: IRQ_ARBITER_INTERFACE, IoConnectInterruptEx, and IoDisconnectInterruptEx.

21. (Original) The system of claim 1, the interrupt is associated with at least one of a local bus, a system bus, a PCI bus, and an ISA bus.

22. (Original) The system of claim 21, the interrupt is at least one of derived from at least two components and coupled to one or more devices that are associated with one or more buses.

23. (Original) The system of claim 21, further comprising at least one bus adaptor to communicate between buses.

24. (Original) The system of claim 1, further comprising at least one local Advanced Programmable Interrupt Controller (APIC) that processes interrupts directed to a processor and an I/O APIC that collects interrupts from devices outside the processor.

25. (Previously Presented) The system of claim 1, further comprising at least one link node to multiplex a plurality of interrupts.

26. (Original) The system of claim 1, further comprising at least one user-mode component and at least one kernel-mode component to arbitrate an interrupt.

27. (Original) A computer readable medium having computer readable instructions stored thereon for implementing the arbiter and processing the request of claim 1.

28. (Currently Amended) A computer implemented method that when executed on one or more processors facilitates managing ~~to manage~~ interrupt resources, comprising:

determining an interrupt range for an interrupt request;

determining an interrupt table entry for the interrupt range;

concurrently assigning the interrupt range and the interrupt table in response to the interrupt request and in view of available system resources, the interrupt request including a requested period of a resource's time to be allocated to a requesting component; and

monitoring system performance and influencing interrupt assignment policy to tune system performance.

29. (Original) The method of claim 28, further comprising determining whether interrupts apply to at least one of an ISA device, a PCI device, and a message-signaled interrupt device.

30. (Original) The method of claim 28, further comprising determining if interrupts are shared by more than one device.

31. (Original) The method of claim 28, further comprising determining whether interrupts are connected to an interrupt controller input directly or to a link node.

32. (Original) The method of claim 28, further comprising matching interrupt properties of at least two devices.

33. (Currently Amended) A system to facilitate interrupt processing, comprising:

means for generating a request for an interrupt resource, the request comprising a requested interval of a resource's time to be allocated to a requesting component;

means for satisfying the request;

means for processing the request as an interrupt assignment and an interrupt table entry;

means for monitoring interrupt resource assignments; and

means for tuning system performance in view of the monitored interrupt resource assignments by adjusting interrupt assignments.

34. (Currently Amended) A computer readable medium having an instruction ~~a data structure~~ stored thereon that when transmitted between two processes executing on one or more processors facilitates interrupt resource assignment, comprising:

a first data field related to a request for an interrupt resource, the request includes at least one interrupt assignment, at least one interrupt table entry associated with the request, and at least one interrupt resource assignment duration to requesting component; and

a second data field related to a resource subset associated with the request.